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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,046	10/28/2003	Takayuki Ito	04329.3167	7595

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EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
03/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/694,046	ITO, TAKAYUKI	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12 and 14-30* is/are pending in the application.

4a) Of the above claim(s) *16-24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-12,14,15 and 25-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

In response to the argument that Paton fails to disclose isolation regions formed in the surface of the substrate, Paton teaches forming FOX or STI regions however does not include these features in the figure. FOX or STI regions are isolation regions formed in the surface of the substrate (FOX or STI "not shown" → Paton, Col. 4 lines 7-14).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1,2,3,4,9,10, 11 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paton et al. (US 6,680,250) in view of Makovicka et al. (2004/0224470 A1).

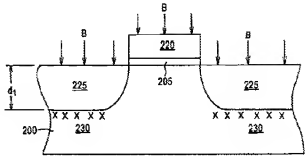

FIG. 2D

Regarding claim 1, Paton in view of Makovicka discloses a method of manufacturing a semiconductor device, comprising:

implanting an electrically inactive first impurity over substantially one entire side of a semiconductor substrate, excluding a region below a gate electrode, to form an implanted layer on an upper portion of the gate electrode and a surface layer of the semiconductor substrate (Paton, Fig. 2D & Col. 4, lines 57-67); and

carrying out heat treatment by light on the side of the semiconductor substrate implanted with the first impurity (Paton, Col. 5 lines 32-34).

Paton does not however explicitly depict providing an "isolation region formed in the surface layer of the semiconductor substrate". Thus in turn can not explicitly disclose wherein the first impurity is implanted into a semiconductor element forming region formed in the surface layer of the semiconductor substrate including the gate electrode, and an upper portion of an isolation region formed in the surface layer of the semiconductor substrate.

Isolation regions formed in the surface layer of the semiconductor substrate are notoriously well known in the art and are an obvious feature when forming a CMOS

semiconductor device such as the device disclosed by Paton. It is known that isolation regions are required adjacent the source/drain in order to provide electrical isolation. Two types of convention isolation regions that perform this function are shallow trench isolation region (STI) and field oxide regions (FOX). These features are conventionally formed prior to forming the gates and implanting. These features are disclosed by Paton but however not depicted. (FOX or STI "not shown" → Paton, Col. 4 lines 7-14). It would be obvious to one of ordinary skill in the art to provide such an isolation structure when forming the device described by Paton. It is obvious that should one of ordinary skill reproduce the process disclosed by Paton and include forming the obviously required isolation regions in the surface of the substrates, it is obvious that the first impurity would also be implanted into the isolation structure along with all of the other features that are exposed on/in the surface of the substrate.

An example of one of ordinary skill in the art disclosing the claimed step of implanting an electrically inactive ion into and also depicting the claimed device structure see Makovicka et al. (2004/0224470 A1). Makovicka et al. disclose forming the CMOS structure as disclosed by Paton including the "isolation regions" formed in the surface of the substrate (See Makovicka et al. figure 2D element [215]. Additionally Makovicka et al. also points out in paragraph [0006] that at the time of the invention it was know to those of ordinary skill in the art to perform a first implant of electronically inactive ions in order to amorphize the surface regions of the silicon substrate which lessens the effects of transient enhanced diffusion (TED).

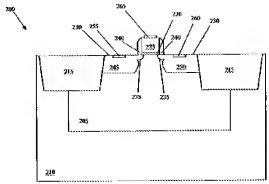

FIGURE 2D

[0006] *Still another way to mitigate TED is to perform an implantation step of implant species that are electrically inactive elements, such as germanium. However, the high doses of germanium needed to amorphize the surface regions of the silicon substrate also damages regions deep within the silicon substrate, creating channels through which boron can diffuse during the thermal anneal. This undesirably results in a shallow junction having a diffuse boundary. Alternatively, low doses of antimony, an electrically active heavy atom (atomic mass unit (AMU) equal to about 122) can be used to localize the damage to surface regions of the substrate.*

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Paton and Makovicka et al to enable the isolation region forming step of Paton to be performed according to the teachings of Makovicka et al because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed isolation region forming step of Paton and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

Regarding claim 2, Paton in view of Makovicka discloses the method according to claim 1, further comprising: implanting electrically active second impurity having predetermined conduction type to the semiconductor substrate before the heat treatment is carried out; and carrying out the heat treatment with respect to the semiconductor substrate to which the first and second impurities are implanted, and thereby, activating the second impurity (Paton, Fig. 2E & Col. 5, line 1+).

Regarding claims 3 and 10, Paton in view of Makovicka teaches the method according to claim 1 and 9 , however does not explicitly disclose the claimed concentration of the first impurity is ion-implanted to the surface layer of the semiconductor substrate. NOTE: Makovicka doe disclose that the implant is at "high doses" in paragraph [0006] and 10^{19} is generally considered a high dosage in the art.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal value for the concentration through routine experimentation and optimization to obtain optimal or desired device performance because the concentration is a result-effective variable and there is no evidence indicating that it is critical or produces any unexpected results and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP § 2144.05

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) "It is not inventive to discover optimum or workable ranges by routine experimentation." Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Any differences in the claimed invention and the prior art may be expected to result in some differences in properties. The issue is whether the properties differ to such an extent that the difference is really unexpected. In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Appplicants have the burden of explaining the data in any declaration they proffer as evidence of non-obviousness. Ex parte Ishizaka, 24 USPQ2d 1621, 1624 (Bd. Pat. App. & Inter. 1992).

An Affidavit or declaration under 37 CFR 1.132 must compare the claimed subject matter with the closest prior art to be effective to rebut a prima facie case of obviousness. In re Burckel, 592 F.2d 1175, 201 USPQ 67 (CCPA 1979).

Regarding claims 4 and 11, Paton in view of Makovicka discloses the method according to claim 1 and 9, wherein at least one of group IV-A elements is used as the first impurity (Paton, Fig. 2D & Col. 4, lines 57-67).

Regarding claim 9, Paton in view of Makovicka discloses a method of manufacturing a semiconductor device, comprising:

providing a gate electrode having a gate insulating film on one main surface of a semiconductor substrate;

entirely implanting electrically inactive first impurity to one main surface of the semiconductor substrate provided with the gate electrode, excluding a region below the gate electrode (Paton, Figs . 1, 2D-F & Cols. 4-5); and

implanting electrically active second impurity having predetermined conduction type to the semiconductor substrate to a region adjacent to the gate electrode of the semiconductor substrate using the gate electrode as a mask (Paton, Figs . 1, 2D-F & Cols. 4-5);

forming shallow source/drain diffusion regions having the predetermined conduction type, the shallow source/drain diffusion regions being formed in a manner that heating treatment using light is carried out with respect to the semiconductor substrate to which the first and second impurities are implanted, and thereby, the second impurity is activated (Paton, Figs . 1, 2D-F & Cols. 4-5);

providing a gate sidewall film around the gate electrode (Paton, Figs . 1, 2D-F & Cols. 4-5);

entirely implanting the first impurity to one main surface of the semiconductor substrate provided with the gate sidewall film , excluding a region below the gate electrode (Paton, Figs . 1, 2D-F & Cols. 4-5); and

implanting the second impurity to the semiconductor substrate to a region adjacent to the gate sidewall film of the semiconductor substrate using the gate electrode and the gate sidewall film as a mask(Paton, Figs . 1, 2D-F & Cols. 4-5); and forming deep source/drain diffusion regions having the predetermined conduction type, and continuing with the shallow source/drain diffusion regions, the deep source/drain diffusion regions being formed in a manner that the heating treatment is carried out with respect to the semiconductor substrate to which the first and second impurities are implanted, and thereby, the second impurity is activated (Paton, Figs . 1, 2D-F & Cols. 4-5).

Paton does not however explicitly depict providing an "isolation region formed in the surface layer of the semiconductor substrate". Thus in turn can not explicitly disclose wherein the first impurity is implanted into a semiconductor element forming region formed in the surface layer of the semiconductor substrate including the gate electrode, and an upper portion of an isolation region formed in the surface layer of the semiconductor substrate.

Isolation regions formed in the surface layer of the semiconductor substrate are notoriously well known in the art and are an obvious feature when forming a CMOS semiconductor device such as the device disclosed by Paton. It is known that isolation

regions are required adjacent the source/drain in order to provide electrical isolation. Two types of convention isolation regions that perform this function are shallow trench isolation region (STI) and field oxide regions (FOX). These features are conventionally formed prior to forming the gates and implanting. These features are disclosed by Paton but however not depicted. (FOX or STI "not shown" → Paton, Col. 4 lines 7-14). It would be obvious to one of ordinary skill in the art to provide such an isolation structure when forming the device described by Paton. It is obvious that should one of ordinary skill reproduce the process disclosed by Paton and include forming the obviously required isolation regions in the surface of the substrates, it is obvious that the first impurity would also be implanted into the isolation structure along with all of the other features that are exposed on/in the surface of the substrate.

An example of one of ordinary skill in the art disclosing the claimed step of implanting an electrically inactive ion into and also depicting the claimed device structure see Makovicka et al. (2004/0224470 A1). Makovicka et al. disclose forming the CMOS structure as disclosed by Paton including the "isolation regions" formed in the surface of the substrate (See Makovicka et al. figure 2D element [215]. Additionally Makovicka et al. also points out in paragraph [0006] that at the time of the invention it was know to those of ordinary skill in the art to perform a first implant of electronically inactive ions in order to amorphize the surface regions of the silicon substrate which lessens the effects of transient enhanced diffusion (TED).

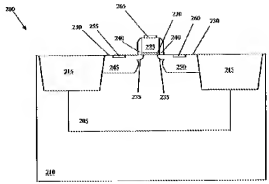

FIGURE 2D

[0006] *Still another way to mitigate TED is to perform an implantation step of implant species that are electrically inactive elements, such as germanium. However, the high doses of germanium needed to amorphize the surface regions of the silicon substrate also damages regions deep within the silicon substrate, creating channels through which boron can diffuse during the thermal anneal. This undesirably results in a shallow junction having a diffuse boundary. Alternatively, low doses of antimony, an electrically active heavy atom (atomic mass unit (AMU) equal to about 122) can be used to localize the damage to surface regions of the substrate.*

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Paton and Makovicka et al to enable the isolation region forming step of Paton to be performed according to the teachings of Makovicka et al because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed isolation region forming step of Paton and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. KSR Int'l Co v. Teleflex Inc.

Regarding claims 27-28, Paton in view of Makovicka teaches the method of claims 1 and 9, wherein the substrate includes isolation regions (STI → Paton, Col. 4 lines 7-14).

Claims 5, 7, 8, 12, 14-15, 25-26 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Paton in view of Makovicka as applied to claims 1-4 above, and further in view of Arai et al (US 4,504,323) and Timans et al (US 6,951,996).

Regarding claims 5 and 12, Paton in view of Makovicka teaches the method according to claim 1 and 9, however does not explicitly disclose pre-heating the semiconductor substrate to predetermined temperature of 600C or less before the heat treatment is carried out with respect thereto; and

carrying out the heat treatment with respect to the semiconductor substrate after pre-heating is made, said pre-heating being flash lamp annealing carried out under conditions that light emitting time is 100 msec or less and irradiation energy density is 100 J/cm^2 or less.

Annealing with a flash lamp was a notoriously well known as an equivalent alternative to laser annealing.

Arai discloses a method for annealing semiconductor devices by means of a flash discharge lamp. Arai teaches a pre-heating step to less that 600 degrees C. Arai also teaches that heating can be done using a xenon lamp or any flash discharge lamps. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the well known and obvious heating techniques as taught by Arai and apply them to the teaching of Paton because they are well known and established alternative to the heat treatment as taught by Paton.

Regarding claims 7- 8 and 14-15, Paton in view of Makovicka in further view of Arai in still further view of Timans teaches the method of claim 5 and 12, but fails to teach carrying out said pre-heating to the semiconductor substrate using at least one of hot plate, heating lamp and laser beams. However, it would have been obvious to one

of ordinary skill in the art at the time the invention was made, to use the lamps as a means for pre-heating the wafer before performing the final anneal using the lamps. See also Timans et al (US 6,951,996) which discusses various pre-heating and heating steps for semiconductor annealing. Choosing and or reordering well known procedures or methods to one of ordinary skill in the art is not inventive. See also Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Regarding claims 25 and 26, Paton in view of Makovicka in further view of Arai in still further view of Timans teaches the method of manufacturing a semiconductor device, comprising:

providing a gate electrode having a gate insulating film on one main surface of a semiconductor substrate;

entirely implanting at least one of a group IV-A element as an electrically inactive first impurity over substantially an entire side of the semiconductor substrate provided with the gate electrode, excluding a region below the gate electrode, to form an implanted layer on an upper portionof the gate electrode and a surface layer of the substrate, and implanting electrically active second impurity having a predetermined conduction type on the semiconductor substrate in a region adjacent to the gate electrode of the semiconductor substrate using the gate electrode as a mask (Paton, Figs . 1, 2D-F & Cols. 4-5); and

forming shallow source/drain diffusion regions having the predetermined conduction type, the shallow source/drain diffusion regions being formed in a manner that heating treatment using light is carried out with respect to the semiconductor substrate to which the first and second impurities are implanted, and thereby, the second impurity is activated (Paton, Figs . 1, 2D-F & Cols. 4-5);

providing a gate sidewall film around the gate electrode (Paton, Figs . 1, 2D-F & Cols. 4-5);

entirely implanting the first impurity to one main surface of the semiconductor substrate provided with the gate sidewall film , excluding a region below the gate electrode (Paton, Figs . 1, 2D-F & Cols. 4-5); and

implanting the second impurity to the semiconductor substrate to a region adjacent to the gate sidewall film of the semiconductor substrate using the gate electrode and the gate sidewall film as a mask(Paton, Figs . 1, 2D-F & Cols. 4-5); and

forming deep source/drain diffusion regions having the predetermined conduction type, and continuing with the shallow source/drain diffusion regions, the deep source/drain diffusion regions being formed in a manner that the heating treatment is carried out with respect to the semiconductor substrate to which the first and second impurities are implanted, and thereby, the second impurity is activated (Paton, Figs . 1, 2D-F & Cols. 4-5).

Paton does not explicitly disclose annealing with a flash lamp and inture the specific wavelength associated to a specific type of lamp. Annealing with a flash lamp was a notoriously well known as an equivalent alternative to laser annealing.

Arai discloses a method for annealing semiconductor devices by means of a flash discharge lamp. Arai teaches a pre-heating step to less that 600 degrees C. Arai also teaches that heating can be done using a xenon lamp or any flash discharge lamps. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the well known and obvious heating techniques as taught by Arai and apply them to the teaching of Paton because they are well known and established alternative to the heat treatment as taught by Paton.

Additionally, it would have been obvious to one of ordinary skill in the art at the time the invention was made, to use the lamps as a means for pre-heating the wafer before performing the final anneal using the lamps. See also Timans et al (US 6,951,996) which discusses various pre-heating and heating steps for semiconductor annealing. Choosing and or reordering well known procedures or methods to one of ordinary skill in the art is not inventive. See also Ex parte Rubin , 128 USPQ 440 (Bd.

App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Paton does not however explicitly depict providing an "isolation region formed in the surface layer of the semiconductor substrate". Thus in turn can not explicitly disclose wherein the first impurity is implanted into a semiconductor element forming region formed in the surface layer of the semiconductor substrate including the gate electrode, and an upper portion of an isolation region formed in the surface layer of the semiconductor substrate.

Isolation regions formed in the surface layer of the semiconductor substrate are notoriously well known in the art and are an obvious feature when forming a CMOS semiconductor device such as the device disclosed by Paton. It is known that isolation regions are required adjacent the source/drain in order to provide electrical isolation. Two types of convention isolation regions that perform this function are shallow trench isolation region (STI) and field oxide regions (FOX). These features are conventionally formed prior to forming the gates and implanting. These features are disclosed by

Paton but however not depicted. (FOX or STI "not shown" → Paton, Col. 4 lines 7-14). It would be obvious to one of ordinary skill in the art to provide such an isolation structure when forming the device described by Paton. It is obvious that should one of ordinary skill reproduce the process disclosed by Paton and include forming the obviously required isolation regions in the surface of the substrates, it is obvious that the first impurity would also be implanted into the isolation structure along with all of the other features that are exposed on/in the surface of the substrate.

An example of one of ordinary skill in the art disclosing the claimed step of implanting an electrically inactive ion into and also depicting the claimed device structure see Makovicka et al. (2004/0224470 A1). Makovicka et al. disclose forming the CMOS structure as disclosed by Paton including the "isolation regions" formed in the surface of the substrate (See Makovicka et al. figure 2D element [215]. Additionally Makovicka et al. also points out in paragraph [0006] that at the time of the invention it was know to those of ordinary skill in the art to perform a first implant of electronically inactive ions in order to amorphize the surface regions of the silicon substrate which lessens the effects of transient enhanced diffusion (TED).

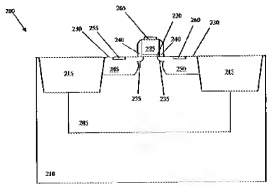

FIGURE 2D

> [0006] *Still another way to mitigate TED is to perform an implantation step of implant species that are electrically inactive elements, such as germanium. However, the high doses of germanium needed to amorphize the surface regions of the silicon substrate also damages regions deep within the silicon substrate, creating channels through which boron can diffuse during the thermal anneal. This undesirably results in a shallow junction having a diffuse boundary. Alternatively, low doses of antimony, an electrically active heavy atom (atomic mass unit (AMU) equal to about 122) can be used to localize the damage to surface regions of the substrate.*

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Paton and Makovicka et al to enable the isolation region forming step of Paton to be performed according to the teachings of Makovicka et al because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed isolation region forming step of Paton and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

Regarding claims 29-30, Paton in view of Arai in view of Timans teaches the method of claims 25 and 26, wherein the substrate includes isolation regions (FOX or STI not shown → Paton, Col. 4 lines 7-14).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando L. Toledo/
Primary Examiner, Art Unit 2823

Jarrett J Stark
Examiner
Art Unit 2823

JJS
February 20, 2008